PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Pai-Hung Pan

Serial No.: 09/072,959

Filed: May 5, 1998

For: TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE

Confirmation No.: 7136

Examiner: G. Fourson III

Group Art Unit: 2823

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APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
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Attn: Board of Patent Appeals and Interferences

Sir:

This Appeal Brief is being submitted in TRIPLICATE pursuant to 37 C.F.R. § 1.192(a) in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c).

(1) REAL PARTY IN INTEREST

U.S. Serial No. 09/172,959, the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc. ("Assignee"). The assignment has been recorded with the United States Patent & Trademark Office ("Office") at Reel No. 8618, Frame No. 0703. Accordingly, Micron Technology, Inc. is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellant nor the undersigned attorney is currently aware of any appeals or interference proceedings that would affect or be affected by the Board's decision in the above-referenced appeal.

(3) STATUS OF CLAIMS

Claims 1-5, 11-17, 25-28, and 33-38 are currently pending and under consideration in the above-referenced application.

No claims have been allowed.

The rejections of claims 1-5, 11-17, 25-28, and 33-38 are being appealed.

(4) STATUS OF AMENDMENTS

The above-referenced application was filed on May 5, 1998, with fifty-two (52) claims. Claims 6-10, 18-24, 29-32, and 39-52, which were already being pursued in a parent of the above-referenced application, were canceled in a Preliminary Amendment that was filed with the above-referenced application.

A first Office Action on the merits was mailed on November 12, 1999.

In response, an Amendment was filed on February 14, 2000.

In view of the arguments that were presented in the Amendment of February 14, 2000, the Office withdrew its previous rejections and presented several new rejections in a second, nonfinal Office Action, which was sent on April 25, 2000.

Another amendment, in which minor revisions were made to the claims merely for the sake of clarity, was filed on July 24, 2000.

In reply, the Office mailed a third, final Office Action on October 11, 2000, maintaining each prior art rejection that was presented in the Office Action of April 25, 2000.

An Amendment Under 37 C.F.R. § 1.116 was filed on December 19, 2000, in which further clarifying amendments were made to the claims.

The Office refused to enter and consider the claim amendments, issuing an Advisory Action on January 4, 2001, in which the latest grounds for rejecting the claims on the basis of subject matter disclosed in the prior art were preserved.

In order to have the claims considered, a Continued Prosecution Application (CPA) was filed on January 11, 2001.

A fourth Office Action on the merits followed on March 30, 2001. In the fourth Office Action, the Office continued to assert each of the previously presented prior art rejections.

On July 2, 2001, another Amendment, in which further clarifications were made in the claims, was filed.

A fifth, final Office Action was mailed on October 11, 2001. Again, the Office maintained each of its previously presented prior art rejections.

Another Amendment Under 37 C.F.R. § 1.116 was mailed on December 11, 2001.

The Office refused to accept the reasoning that was presented in the December 11, 2001, Amendment Under 37 C.F.R. § 1.116, issuing an Advisory Action on January 7, 2002.

Thereafter, on January 16, 2002, a Request for Continued Examination (RCE) was filed.

On April 9, 2002, the Office mailed a sixth Office Action, in which claims 11-17 and 33-38 were allowed. The prior art rejections of the remaining claims were, however, maintained.

Further explanations as to the patentability of the claims that remained rejected were provided in a Response dated July 16, 2002.

A seventh, nonfinal Office Action was sent on October 24, 2002. The Office withdraw its allowance of claims 11-17 and 33-38, reinstating its prior art rejections of these claims and maintaining each of the prior art rejections that remained.

On January 29, 2003, another Amendment was filed. A few more minor claim amendments were presented to further clarify the subject matter that was already recited in the amended claims. In addition, reasoning was provided to clearly explain the patentability of each of the pending claims.

Nonetheless, each of the pending claims was again rejected in an eighth, final Office Action dated April 8, 2003. Again, the Office asserted each of the prior art rejections that it had been asserting since April 25, 2000.

In a Response to the Final Office Action, which was filed on June 13, 2003, a final effort was made to convince the Office that each of claims 1-5, 11-17, 25-28, and 33-38 recites subject

matter which is allowable over the prior art that has been made of record in the above-referenced application.

In an Advisory Action dated July 15, 2003, the Office indicated its intent to continue its refusal to accept the explanations of patentability.

Accordingly, a Notice of Appeal was filed on July 18, 2003.

This Appeal Brief follows the Notice of Appeal.

(5) SUMMARY OF THE INVENTION

The above-referenced application teaches a method for forming an isolation structure for a semiconductor device. In the method, a layered structure which includes a semiconductor substrate, a dielectric layer, and a buffer film layer is provided. Fig. 1; page 4, lines 13-22; page 6, lines 15-25. The layered structure is then etched to define a trench which extends through the buffer film layer, through the dielectric layer, and into the semiconductor substrate. Figs. 2 through 4; page. 4, lines 23-27; page 6, line 26, to page 7, line 7. The trench has sidewalls and a bottom. *See, e.g.,* Fig. 4.

An oxide layer is then formed on portions of the semiconductor substrate that are exposed within the trench. Fig. 5; page 5, lines 1-3; page 7, lines 8-11. Thermal oxidation processes may be used to form the oxide layer. Page 5, lines 1-3; page 7, lines 8-11.

A portion of the buffer film layer is selectively etched. Fig. 6; page 5, lines 3-5; page 7, lines 11-16. Such selective etching may expose portions of an upper surface of the dielectric layer that are located adjacent to an upper edge of the trench. *See* Fig. 6. Some of the buffer film layer remains on the semiconductor substrate following such selective etching. *See id.*

Isolation material is applied over the buffer film layer, with major surfaces of the applied layer of isolation material and the buffer film layer in contact. Fig. 7; page 5, lines 17-19; page 7, lines 17-21. The isolation material also fills the trench. *See id.* The isolation material may be annealed to densify the same. Page 5, lines 19-21; page 7, lines 21-26.

Thereafter, a portion of the isolation material layer that is located above the buffer film layer is removed. Fig. 8; page 5, lines 21-25; page 7, line 27, to page 8, line 1. The buffer film layer is also removed. Fig. 9; page 5, lines 25-26; page 8, lines 1-3. The isolation material forms a shallow trench isolation (STI) structure which has a capped appearance. *See* Fig. 10; page 5, line 26, to page 6, line 2; page 8, lines 3-7. The capped portion of the STI structure may extend over an upper surface of the semiconductor substrate, for example, a distance of about 50 Å to about 150 Å. Page 8, lines 7-9.

(6) ISSUES

(A) Whether claims 1-4, 11-14, 16, 25-27, 33-35, and 37 recite subject matter which is patentable under 35 U.S.C. § 102(e) over the subject matter described in U.S. Patent 5,712,185 to Tsai et al. (hereinafter "Tsai");

(B) Whether claims 17 and 38 are patentable under 35 U.S.C. § 103(a) for reciting subject matter which is nonobvious over that taught in Tsai and the Examiner's Comment; and

(C) Whether claims 5, 15, 28, and 36 are patentable under 35 U.S.C. § 103(a) for reciting subject matter which is allowable over that taught in Tsai, in view of teachings from Lee HS, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench

Isolation (STI)," 1996 IEEE Symposium on VLSI Technol. Dig. of Technical Papers, pages 158-59 (hereinafter "Lee").

(7) GROUPING OF CLAIMS

Claims 1-5, 11-17, 25-28, and 33-38 should be grouped together. Of these, claim 25 appears to be the most generic. Claims 1-5, 11-17, 26-28, and 33-38 stand and fall with claim 25.

(8) ARGUMENT

(A) Rejections Under 35 U.S.C. § 102(e)

Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Tsai.

(i) Applicable Law

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

(ii) Reference Relied Upon

Tsai

Tsai describes a method for forming shallow trench isolation structures in a semiconductor substrate. The method of Tsai includes providing a substrate 30 that includes a silicon oxide layer, which is referred to as "pad oxide layer 32," thereover, as well as a silicon nitride layer 34 over the pad oxide layer 32. FIG. 3A; col. 2, lines 53-58. A sacrificial layer 36 of either polysilicon or silicon oxide is formed over the silicon nitride layer 34. FIG. 3B; col. 2, line 59, to col. 3, line 2. A photomask 37 with apertures for defining trenches in the semiconductor substrate 30 is then formed over the sacrificial layer 36. FIG. 3C; col. 3, lines 3-4. Next, the trenches 38 are formed through each of layers 36, 34, and 32 and in the semiconductor substrate 30. FIG. 3D; col. 3, lines 19-23.

The photomask 37 is then removed and the silicon nitride layer 34A descumed, or etched laterally beneath the overlying sacrificial layer 36A. FIG. 3E; col. 3, lines 19-23.

A thin oxide layer 39 is then formed on the surfaces of the semiconductor substrate 30 that are exposed within the trench 38A. FIG. 3F; col. 3, lines 34-38.

The trench 38A is filled with a suitable dielectric material, which is referred to as "isolation material 40," such as tetraethylorthosilicate (TEOS), which also fills the descumed regions of the silicon nitride layer 34B and forms a dielectric layer over the sacrificial layer 36A. FIG. 3G; col. 3, lines 38-50.

The dielectric layer and sacrificial layer 36A are then removed to expose the surface of the silicon nitride layer 34B and to form an isolation region 40A from the isolation material. FIG. 3H; col. 3, lines 51-56. Upon removal of the silicon nitride layer 34B, regions of the

dielectric material that filled the descumed portion of the silicon nitride layer 34B extend laterally beyond the outer periphery of the trench 38A and over portions of the pad oxide layer 32A. FIG. 3I; col. 3, lines 57-60. Exposed portions of the pad oxide layer 32A are then removed from the surface of the semiconductor substrate 30, leaving only the isolation region 40A and portions of the pad oxide layer 32B that are shielded thereby. FIG. 3J; col. 3, lines 60-66.

(iii) Analysis

In contrast to the method disclosed in Tsai, each of independent claims 1, 11, 25, and 33 recites a method of forming an isolation structure which includes applying a layer of isolation material "over [a] buffer film layer, [with] major surfaces of [the] layer of isolation material and [the] buffer film layer in contact . . ."

The third edition of the American Heritage College Dictionary defines "major" as "great in scope or effect." The definition for "major" that has been cited by the Office is similar, "notable or conspicuous in effect or scope." It appears, however, that the Office has not considered the magnitude identified by the terms "notable" and "conspicuous." "Notable" is defined by the third edition of the American Heritage College Dictionary as meaning "[w]orth of note or notice; remarkable . . .," as well as "[c]haracterized by excellence or distinction . . ." That dictionary defines the term "conspicuous" as "[e]asy to notice; obvious . . ."

It is respectfully submitted that the 1,000 Å (0.1 μm) to 5,000 Å (0.5 μm) edge of the silicon nitride layer 34 of Tsai is not "major," "great," "notable," or "conspicuous" in scope relative to the distance (typically several microns) across the area between adjacent isolation

regions and, thus, the dimensions across the upper and lower *surfaces* thereof. As such, one of ordinary skill in the art would readily recognize that the term "major surface" does not apply to the extremely thin edges of the silicon nitride layer 34 but, rather, to the *surfaces* (*i.e.,* upper and lower surfaces) thereof.

FIG. 3G of Tsai clearly illustrates that a major surface of the isolation material 40, when applied, contacts a major surface of the sacrificial layer 36A, which is formed from either polysilicon or silicon oxide, not from silicon nitride. Col. 2, line 59, to col. 3, line 2. Thus, Tsai does not expressly or inherently describe that the major surface of the isolation material 40 contacts the major surface of the silicon nitride layer 34, as required by each of independent claims 1, 11, 25, and 33.

Therefore, Tsai does not anticipate any of independent claims 1, 11, 25, or 33 under 35 U.S.C. § 102(e). Accordingly, under 35 U.S.C. § 102(e), each of independent claims 1, 11, 25, and 33 is allowable over Tsai.

Claims 2-4 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Each of claims 12-14 and 16 is allowable, among other reasons, for depending either directly or indirectly from claim 11, which is allowable.

Claims 26 and 27 are both allowable, among other reasons, for respectively depending directly and indirectly from claim 25, which is allowable.

Claims 34, 35, and 37 are each allowable, among other reasons, as depending either directly or indirectly from claim 33, which is allowable.

In view of the foregoing, reversal of the 35 U.S.C. § 102(e) rejections of claims 1-4, 11-14, 16, 25-27, 33-35, and 37 is respectfully requested.

(B) Rejections Under 35 U.S.C. § 103(a)

Claims 5, 15, 17, 28, 36, and 38 stand rejected under 35 U.S.C. § 103(a).

Tsai

Claims 17 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of the Examiner's Comment.

Claim 17 is allowable, among other reasons, for depending from claim 11, which is allowable.

Claim 38 is allowable, among other reasons, for depending from claim 33, which is allowable.

Tsai in View of Lee

Claims 5, 15, 28, and 36 each stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of Lee HS, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)," 1996 IEEE Symposium on VLSI Technol. Dig. of Technical Papers, pages 158-59 (hereinafter "Lee").

Claims 5, 15, 28, and 36 are each allowable, among other reasons, for depending from claims 1, 11, 25, and 33, respectively, each of which is allowable.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 5, 15, 17, 28, 36, and 38 be reversed.

(9) APPENDIX

A copy of claims 1-4, 11-14, 16, 25-27, 33-35, and 37 as last amended is appended hereto as the "Appendix."

(10) CONCLUSION

It is respectfully submitted that:

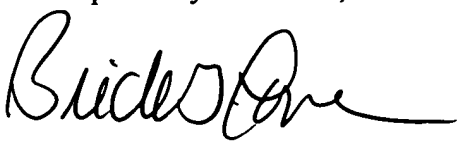
(A) Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 recite subject matter which is patentable under 35 U.S.C. § 102(e) over the subject matter described in Tsai;

(B) Claims 17 and 38 are patentable under 35 U.S.C. § 103(a) for reciting subject matter which is nonobvious over that taught in Tsai and in consideration of the Examiner's Comment; and

(C) Claims 5, 15, 28, and 36 are allowable under 35 U.S.C. § 103(a) for reciting subject matter which is patentable over that taught in Tsai, in view of teachings from Lee.

Accordingly, it is respectfully requested that the rejections of claims 1-5, 11-17, 25-28, and 33-38 be reversed and that each of these claims be allowed.

Respectfully submitted,



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APPENDIX

CLAIMS

1. A method of forming an isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer, with major surfaces of said layer of isolation material and said buffer film layer in contact, and filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

2. The method of claim 1, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

3. The method of claim 1, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

4. The method of claim 3, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

5. The method of claim 1, further including annealing said isolation material layer.

11. A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer to expose portions of an upper surface of said dielectric layer adjacent to an upper edge of said trench;

applying a layer of isolation material over said buffer film layer, with major surfaces of said layer of isolation material and said buffer film layer in contact, said isolation material also substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

12. The method of claim 11, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

13. The method of claim 11, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

14. The method of claim 13, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

15. The method of claim 11, further including annealing said isolation material layer.

16. The method of claim 11, wherein said capped shallow trench isolation structure includes ledges which extend a distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

17. The method of claim 16, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.

25. A method of forming an isolation structure on a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench extending through said buffer film layer and said dielectric layer and into said semiconductor substrate, and an oxide layer located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer, major surfaces of said layer of isolation material and said buffer film layer in contact, said isolation material substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

26. The method of claim 25, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

27. The method of claim 26, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

28. The method of claim 25, further including annealing said isolation material layer.

33. A method of forming a capped shallow trench isolation structure for a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench extending through said buffer film layer and said dielectric layer and into said semiconductor substrate, and an oxide layer located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer to expose portions of an upper surface of said dielectric layer adjacent an upper edge of said trench;

applying a layer of isolation material over said buffer film layer, with major surfaces of said layer of isolation material and said buffer film layer in contact, said isolation material substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

34. The method of claim 33, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

35. The method of claim 34, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

36. The method of claim 33, further including annealing said isolation material layer.

37. The method of claim 33, wherein said capped shallow trench isolation structure includes ledges which extend a distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

38. The method of claim 37, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.